Specification Amendments

Please replace the corresponding original parts with the amended parts provided below.

BACKGROUND OF THE INVENTION

Field of the Invention

This invention is directed to an analysis of a waveform for a telecommunication system or for a measurement equipment, and more particularly to a Digital Signal Processing of Multi-Sampled Phase (DSP MSP).

The DSP MSP allows waveform analysis, noise filtering, and data recovery for wireless, optical , or wireline transmission systems and measurement systems and for a wide range of data rates and waveform timings.

The invention further includes Sequential Data Recovery from Multi Sampled Phase (SDR MSP), which is a version of the DSP MSP, which provides clock and data recovery for optical communications.

Background Art

Background art for this invention is represented by the documents listed below:

D1 (US 5,668,830 by Georgiu Christos John ET AL)

D2 (PCT/CA01/00723 invented by Bogdan);

D3 (US 2002/0009171 invented by Ribo);

D4 (US 5,592,125 invented by Williams).

The D1 is limited to using delay lines and most basic digital filters for removing phase noise of waveform edges. D1 circuits enable merely edge phase aligning and data re-timing on a bit per bit basis for data serializing/de-serializing only.

Consequently, D1 circuits do not have any of the fundamental features of the present invention such as; over-sampling and noise filtering from entire pulse necessary for elimination of noise occurring inside data pulses, or cumulative processing operations necessary for measuring and processing lengths of transmitted pulses, or adaptive signal processing using wave-form

screening.

The D2 solution created variety of high resolution phase capturing techniques which are useful for measuring phase skews between low frequency frames in high quality synchronization circuits.
However these D2 phase capturing techniques have never been targeting any processing throughput which could be even close to that needed for communication signal processing.
Therefore besides said high resolution phase capture, the D2 solution has fundamentally different principle of operation and produces entirely different results.
Consequently D2 can not contribute to any processing of much higher frequency signals commonly used in communication links.

The D3 solution represents latest generation of clock and data recovery (CDR) circuits which over-sample in expected transition region in order to achieve some fractional improvements of jitter tolerance.
The D3 captures windows consisting of samples covering entire data bit interval.
Every such window covers single bit interval only and it is captured and processed separately from other windows on a bit interval by bit interval basis without any correlation between data captured in consecutive windows. Such lack of correlation amounts to inability to filter out narrow glitches occurring between windows.
Therefore the D3 windows need to be centered around expected edges of received data bits in order to enable said bit by bit processing without data recovery errors.
Obviously such window centering can only be achieved by phase locking to the received signal.

Other over-sampling solution is the CDR with bang-bang phase detector (CDR with BBPD) represented by D4.
While taking more samples provides D3 with better base for jitter filtering than that of the CDR with BBPD, dynamics of D3 phase locking has to accommodate additional interference caused by said jiter filtering and by further processing of output data providing return reference for the D3 phase locked loop.
Similarly as the D3 and the CDR with BBPD, all other conventional analyzers and receivers of serial data have the same common feature limiting severely their performances; they require phase locking to

received signal in order to recover data based on sampling localized in a credible region of the received wave-form.

The phase locking requirement is not only difficult to achieve but furthermore it imposes significant limitations on receiver performances such as those listed below:

- Jitter tolerance is very low outside the bandwidth of receivers PLL while such PLLs bandwidth is usually below 1/10 of the bandwidth of transmitted signals which are the major sources of phase jitter and amplitude noise.
- Such receivers are defenseless against high frequency noise occurring in wave-form regions which can not be filtered out using said localized sampling.
- Such PLL based receivers require significant lock acquisition times before newly established data link becomes operational what is an impediment for all burst types of data links.

This invention is based on fundamentally different principle of operation relying on; measurements of pulse lengths of incoming wave-form with accuracy matching single gate delays, and on digital processing of such accurate pulse lengths in order to recover data transmitted by the wave-form or to analyze the waveform.

Such superior principle of operation combined with adaptive signal processing algorithms utilizing verification of received waveforms, eliminate all the above deficiencies of the conventional solutions and enable significantly longer transmission distances.

SUMMARY OF THE INVENTION

1. Purpose of the invention

It is an object of present invention to create a circuit for Digital Signal Processing of Multi-Sampled Phase (DSP MSP) comprising circuits for Sequential Data Recovery from Multi Sampled Phase (SDR MSP) of an optically received wave-form.

The DSP MSP shall allow programmable comprehensive noise filtering and wave-form timing analysis for wave-forms ranging from lowest to highest frequencies.

The DSP MSP allows waveform analysis, noise filtering, and data recovery for wireless, optical , or wireline transmission systems and measurement systems.

Specification Pages Amendments

Please replace the original page 11 of the Specification with the amended page 11 provided below:

In addition to the outputs of the digital filter arithmometers 11DFA1/12DFA1 of the phases 11/12: several carry over bits (22DFR(Cov)/21DFR(Cov)) from the registers of the previous parallel phases 22/21, are re-timed into the digital filter registers 11DFR/12DFR by the clocks 11Clk1/12Clk1.
Similarly carry over bits (11DFR(Cov)/12DFR(Cov)) from the registers of the phases 11/12, are re-timed into the digital filter registers 21DFR/22DFR.
Said carry over bits from the previous parallel phases allow the next third stage of the SDR MSP to filter incoming wave-form pulses which extend beyond a boundary of a single capture register.

The 11DFR/12DFR are connected to the digital filter arithmometers 11DFA2/12DFA2 (see FIG. 3A), which are both fed to the digital filter register (1DFR) through the 2:1 selector (2:1SEL).
Similarly as for said second stage:
The programmable control unit (PCU) determines logical and/or arithmetical processing which the 11DFA2/12DFA2 shall perform, by pre-loading the filter control register (FCR2) with a control code which is applied to the 11DFA2/12DFA2.
Additionally the PCU determines the mask FMR2(R:0) which the pre-filtered data 11DFR/12DFR shall be processed against, by pre-loading the filter mask register (FMR2).

The 11SEL signal equal to 1/0 selects the 11DFA2(R:0)/12DFA2(R:0), to be downloaded to the phase one digital filter register (1DFR) by the clock 1Clk2 (see FIG.3A and FIG.2A).

4. Sequential Phase Control and Phase Processing Stages

The Sequential Phase Control is shown in the FIG.2B and the Phase1 Processing Stages 2 to 8 (1PPS) are shown in the FIG.3A.
The binary edge encoders (BEE) are implemented by the third stage of the SDR MSP, in order to convert filtered sampling data into binary encoded transition time of the filtered MW signal.
The phase1 front edge encoder (1FEE) detects a last transition of the MW during the sampling

period, and produces a binary number of sampling clocks which occurred between the beginning of the sampling period and the last transition.

The phase1 end edge encoder (1EEE) detects a first transition of the MW during the sampling period, and produces a binary number of sampling clocks between the beginning of the sampling period and the first transition.

Whenever only one transition of the MW occurs during a sampling period (Ps), a difference of the 1FEE minus the 1EEE shall amount to 0.

If two transitions of the MW occur, the difference of the 1FEE minus the 1EEE shall amount to a positive nonzero number of sampling clocks which occurred between the transitions.

Please replace the original page 16 of the Specification with the amended page 16 provided below:

- a data bit is added to a data string which corresponds to the MW inter-transition interval (see Sec. "Received Data Collection");
- a phase skew, which is expected between a sampling clock period and a period of a received data bit, is added to the phase1 skew accumulator1 (1PSA1) as it is further explained in the Sec. "Periodical Skew Accumulation".

While the above mentioned functions are being performed by the Received Data Collection and by the Periodical Skew Accumulation, outputs of the Phase Processing Stages (see FIG.3A) are ignored until the end of the string.

In order to explain operations of the Phase Processing Stages at the end of a data string, listed below estimates shall be made:

- the content of the above mentioned 1ESR2 never exceeds +/- Ps (where Ps is a sampling clock period), because the 1FER and 1EER can never exceed 1Ps value and the 1ESR2 is loaded with their subtraction result;
- the content of the 1PSA1 never exceeds +/- 1.2Ps, because eventual positive/negative 1PSA1 overflows are corrected by subtracting/adding an expected data bit period and increasing/decreasing number of data bits which are being collected.

When the end of the string is reached, the Phase Processing Stages perform functions which are explained below.

The 1FER is subtracted form the 1EER and the resulting phase skew between the front and end edges is transferred into the phase1 edge skew register2 (1ESR2).

The 1PSA1 and the 1ESR2 are added and the result, which is not greater than 2.2Ps, is loaded into the phase1 final skew register (1FSR).

The 1FSR content is evaluated for how many received data bits it corresponds to and used to modify lengths of the data string, as it is further explained below.

If 1FSR(P) = 1 indicates positive 1FSR content: 1FSR - 1.5Pe is loaded into the phase1 double length register (1DLR), and 1FSR - 0.5Pe is loaded into the phase1 single length register (1SLR)

(where the Pe is an averaged expected data bit period which is calculated and provided by the PCU).

A positive 1DLR content indicated by the 1DLR(P) = 1, shows that the 1FSR content shall be approximated to +2 data bits which need to be added to the data string by the Data Collection circuits.

A negative 1DLR content indicated by the 1DLR(P) = 0 and a positive 1SLR content indicated by the 1SLR(P) = 1, show that the 1FSR content shall be approximated to +1 data bits which need to be added to the data string by the Data Collection circuits.

When the 1SLR is negative, the 1SLR(P) = 0 indicates that the 1FSR content shall be approximated to 0 data bits and nothing is added to the data string by the Data Collection circuits.

If 1FSR(P) = 0 indicates negative 1FSR content: 1FSR + 1.5Pe is loaded into the phase1 double length register (1DLR), and 1FSR + 0.5Pe is loaded into the phase1 single length register (1SLR).

A negative 1DLR content indicated by the 1DLR(P) = 0, shows that the 1FSR content shall be approximated to -2 data bits and 2bits need to be subtracted from

Please replace the original page 29 of the Specification with the amended page 29 provided below:

At the beginning of the next time frame, which has 128 phase1 cycles, the last captured 1DDB content is further downloaded to the phase1 data register (1DDR) by the clock signal 1Clk3/128. Number of said mask detections is counted in the mask counter buffer (1MCB), as it is explained below:

- at the beginning of every time frame which has 128 phase1 cycles, the 1MCB is reset/preset to 0/1 if there isn't/is a mask detection for the first cycle of the frame which is signaled by the 1PHA/128ena = 1;
- the 1MCB is increased by 1 / kept the same, if there is / isn't any mask detection during a particular phase1 cycle;
- at the beginning of the next time frame, the 1MCB is downloaded to the phase1 mask counter register (1MCR) and the output of the 1MCB>0 decoder (MCB>0 DEC) is downloaded to the 1MCR(P) bit, by the 1Clk3/128.

Said 1DDR and 1MCR are read by the PCU, when the beginning of the next frame is communicated to the PCU by the phase1 128th clock enable signal (1PHA/128ena) and the above mentioned 1MCR(P) = 1 indicates that at least 1 detection of a pre-selected mask occurred during the previous frame.

Said PCU controlled capturing of a wave buffer content is implemented, as it is explained further below.

The sample number register (SNR) is loaded by the PCU: with a phase number defined as phase1/phase2 if the SNR(0) is set 0/1, and with a particular phase cycle number in a time frame defined by SNR(7:1) bits.

Since there are 2 phases with 128 cycles per time frame, SNR(7:0) bits define 1 of 256 sampling cycles for having its wave buffer captured and made available for a further analysis by the PCU.

Said SNR is downloaded into the phase1 sample number buffer (1SNB) at the beginning of a time frame by the first phase1 clock of the frame 1Clk2/128.

At the beginning of a time frame: the phase1 sample number counter (1SNC) is set to 0, since the 1PHA/128ena selects 0 to be loaded into the 1SNC by 1Clk2.

During every other cycle of the time frame: 1 is added to the SNC content, since the 1PHA/128ena

is inactive during all the next cycles of the frame.

The 1SNC(7:1) and the 1SNB(7:1) are being compared by the logical comparator (Log.Comp.), which produces the Eq = 1 signal when their identity is detected.

Said Eq = 1 enables the 1SNB(1) = 0/1 to select the 11WB(R:0)/12WB(R:0) in the 3:1 selector (3:1 SEL), for capturing in the phase1 sampled data buffer (1SDB).

At the beginning of the next time frame, the output of the 3:1 SEL is additionally captured in the phase1 sampled data register (1SDR) by the signal 1Clk3/128.

Said 1SDR is read by the PCU, which is notified about availability of the requested sample by the signal 1PHA/128ena.

CONCLUSION

In view of the above description of the invention and associated drawings, other modifications and variations will now become apparent to those skilled in the art based on the teachings contained herein. Such other modifications and variations fall within the scope and spirit of the present invention.